ACSP · Analog Circuits and Signal Processing

Pieter A. J. Nuyts Patrick Reynaert Wim Dehaene

Continuous-Time Digital Front-Ends for Multistandard Wireless Transmission

Analog Circuits and Signal Processing

Series editors

Mohammed Ismail, Dublin, USA Mohamad Sawan, Montreal, Canada

For further volumes: <http://www.springer.com/series/7381> Pieter A. J. Nuyts • Patrick Reynaert Wim Dehaene

Continuous-Time Digital Front-Ends for Multistandard Wireless Transmission

Pieter A. J. Nuyts Tri ICT Zaventem Belgium

and

ESAT-MICAS KU Leuven Leuven Belgium

Patrick Reynaert ESAT-MICAS KU Leuven Leuven Belgium

Wim Dehaene ESAT-MICAS KU Leuven Leuven Belgium

ISSN 1872-082X
ISSN 2197-1854 (electronic)
ISBN 978-3-319-03925-1 (eE ISBN 978-3-319-03925-1 (eBook) DOI 10.1007/978-3-319-03925-1 Springer Cham Heidelberg New York Dordrecht London

Library of Congress Control Number: 2013956436

- Springer International Publishing Switzerland 2014

This work is subject to copyright. All rights are reserved by the Publisher, whether the whole or part of the material is concerned, specifically the rights of translation, reprinting, reuse of illustrations, recitation, broadcasting, reproduction on microfilms or in any other physical way, and transmission or information storage and retrieval, electronic adaptation, computer software, or by similar or dissimilar methodology now known or hereafter developed. Exempted from this legal reservation are brief excerpts in connection with reviews or scholarly analysis or material supplied specifically for the purpose of being entered and executed on a computer system, for exclusive use by the purchaser of the work. Duplication of this publication or parts thereof is permitted only under the provisions of the Copyright Law of the Publisher's location, in its current version, and permission for use must always be obtained from Springer. Permissions for use may be obtained through RightsLink at the Copyright Clearance Center. Violations are liable to prosecution under the respective Copyright Law. The use of general descriptive names, registered names, trademarks, service marks, etc. in this publication does not imply, even in the absence of a specific statement, that such names are exempt from the relevant protective laws and regulations and therefore free for general use.

While the advice and information in this book are believed to be true and accurate at the date of publication, neither the authors nor the editors nor the publisher can accept any legal responsibility for any errors or omissions that may be made. The publisher makes no warranty, express or implied, with respect to the material contained herein.

Printed on acid-free paper

Springer is part of Springer Science+Business Media (www.springer.com)

To Ineke My friend, my love, my companion

Preface

The book you're holding, physically or electronically, is the result of a very interesting, challenging but also rewarding research project. The research was carried out in different contexts and cooperations but it was centered around the following question: how can we make the RF transmitters of our modern communication systems (WiFi, GSM, LTE, and so on) more flexible and more efficient at the same time. We engaged on a digitalization route to realize this. What this means in terms of digital modulation is the subject of this book. This modulation problem is treated in many of its dimensions: we make high-level system considerations, go through the system's mathematics, and proceed all the way down to implementation in 65 and 40 nm standard CMOS.

You read this well. There are a lot of different abstraction levels in this book. It is our strong belief that this is the only way to come to optimal solutions. Keep the different abstractions in place to handle complexity. However, try to think as much as possible across the levels to find the co-optimization opportunities. For the topic of digital RF, anything else simply does not make sense. What may look mathematically very attractive is not always implementable. Straightforward implementations often don't meet the performance requirements. System-circuit co-design is the answer in that case. Also RF-PA and digital modulator co-design is required. We set first steps in this.

Research these days is per definition collaborative: Ph.D. students interact with their advisors, together they interact with interested industrial partners, and so on. Only when there is sufficient match in these interactions, the research outcome will be both scientifically relevant and industrially applicable. In this context, the authors would like to thank Franz Dielacher and Peter Singerl from Infineon Austria for their continuous support and belief in our work. Even when the work was rather academic or heavily mathematical they kept up the encouragement and made us go on in the direction needed in their industrial applications. This cooperation was essential in the realization of the results we are presenting in this manuscript. Special thanks also go to Brecht François for his cooperation in making the link with the domain of RF power amplification.

Dear reader, we hope you enjoy reading this book as much as we enjoyed the research that led to it.

Leuven, October 2013 Wim Dehaene

Pieter A. J. Nuyts Patrick Reynaert

Contents

Symbols

Non-alphanumerical Symbols and Operators

Functions and Operators

Signals and Their Spectra

Other Symbols

- τ_n Propagation delay of the *n*th delay element in a delay line
- τ_u Unit delay in a delay line
 φ Phase
- Phase

Acronyms

Chapter 1 Introduction

1.1 Situation and Motivation

Wireless communication technology is constantly gaining importance. Through the availability of affordable laptops and certainly cell phones and smart phones, it now plays an important role in the daily life of billions of people. In 2007, the number of cell phone subscribers worldwide was estimated to be about 3.3 billion or about 49 % of the Earth's population [\[6](#page--1-1), [23\]](#page--1-2), and in Europe there even were more cell phone subscriptions than people, with about 1.1 subscription per person [\[6\]](#page--1-1). During 2007, 1.2 billion cell phones were sold worldwide [\[19\]](#page--1-3).

In addition to basic cell phones (so called *feature phones*), smart phones are steadily becoming more powerful and more popular. In 2007, for the first time more smart phones than laptops were sold worldwide [\[19](#page--1-3)] with a year total of 116 million smart phones. Back then, forecasts predicted around 500 million smart phones for 2013 [\[19](#page--1-3)], but at the beginning of 2013, almost 920 million smart phones are expected to be sold throughout the year, which means that for the first time smart phone sales will surpass those of feature phones [\[12\]](#page--1-4). Current forecasts [\[12](#page--1-4)] predict 1.5 billion smartphones being sold during 2017, which would be about 2/3 of the total cell phone market.

While the number of users keeps growing, users also transmit increasing amounts of data year after year. To accommodate for this, new communication standards emerge constantly in order to achieve higher data rates and accommodate new types of functionality. Furthermore, new frequency ranges are regularly allocated to increase the amount of data that can be transmitted and to allow multiple standards to coexist without interfering.

Modern advanced wireless devices, such as smart phones or tablet computers often support multiple communication standards such as GSM, UMTS (3G), LTE (4G), wireless LAN (WLAN), Bluetooth, GPS, etc. For historical reasons, the same standards often use different frequency bands in different geographical regions. A good example of this is the GSM standard for mobile telephony, which operates at 900 and 1800 MHz in most of Africa, Europe and Asia, but at 850 and 1900 MHz in Canada and the USA [\[20](#page--1-5), [21](#page--1-6)]. This means that even a basic European cell phone needs to support two frequency bands, and in order to also have coverage in North-America, three or four bands are required. Clearly, more advanced devices need to support even more frequency bands. In addition to this, wireless devices need to be limited in size and cost and must be efficient in terms of power consumption in order to have a long battery lifetime.

Different standards impose entirely different specifications on a device. For example, GSM devices may need to transmit relatively high output power (up to 2 W [\[20\]](#page--1-5)) in order to reach the nearest base station which in rural areas might be several kilometers away. Meanwhile, the required data rate is only about 270 kbit/s [\[20](#page--1-5)] since only a voice signal needs to be transmitted. A WLAN transmitter, on the other hand, needs much lower output power since the WLAN modem is usually located within tens of meters from the transmitter, but has to achieve very high data rates (currently tens to hundreds of Mbit/s [\[22\]](#page--1-7)) in order to provide a fast internet connection. Therefore, WLAN transmitters need much more accurate modulators than GSM transmitters. Because of these differences as well as the different frequency bands, optimal transmitters and receivers for different standards can be very different.

This can be solved by including a separate chip for every communication standard. However, this makes the devices large and expensive and requires separate chips to be designed every time a new communication standard appears. It would be more convenient if a single chip could be designed that can be reconfigured to meet the specifications of different standards. This requires less area and results in reduced design and production costs. Furthermore, in the ideal case, new standards can be added simply by modifying the software in order to configure the chip in a different way. This is called *software radio* (SR) or *software-defined radio* (SDR) depending on the degree of flexibility (see below).

The subject of this book is situated in the area of single-chip multistandard transceivers. Most wireless devices include both transmitters and receivers in order to transfer information in both directions (a notable exception is, for example, a GPS receiver which does not need to transmit any information). While the concepts of SDR and SR apply to both transmitters and receivers, this book focuses on the transmitter, and more specifically, on the *RF front-end*. This is the part that produces the transmitted radio frequency (RF) signals.

In the following sections, different aspects of modern wireless transmitters are discussed. It will be shown that the required flexibility is best achieved by implementing as many components as possible using digital circuits, which can be reconfigured more easily. More specifically, this book aims at removing the digital-to-analog converters and analog mixers which are typically present in traditional transmitter front-ends. This can be done by using *switched-mode power amplifiers*, which can be driven directly by digital circuits, and which furthermore are more efficient than traditional linear amplifiers. In addition to being flexible and efficient, this type of transmitters is more suited to be implemented on-chip in nanoscale CMOS technologies, which is important in order to reduce their cost and size.

This way, the subject of this book will be defined to be the design of efficient fully integrated, fully digital multistandard RF transmitter front-ends in nanoscale CMOS. The state of the art in this area will be examined in Chap. [2,](http://dx.doi.org/10.1007/978-3-319-03925-1_2) after which it is advanced in the following chapters.

1.1.1 Towards Software-Defined Radio

Figure [1.1](#page-24-1) shows a traditional transmitter for a single digital standard. The input is a stream of data bits, which are a digital representation of some type of information that needs to be transmitted, e.g. a voice or video signal, a picture, an e-mail, etc. A *digital signal processing* (DSP) block converts the bits to a digital baseband signal suitable for wireless transmission (more information about this conversion, called *modulation*, is given in Sect. [2.1\)](http://dx.doi.org/10.1007/978-3-319-03925-1_2). This digital baseband signal is converted to an analog signal using a *digital-to-analog converter* (DAC). A lowpass filter (LPF) removes the spectral replicas created by the DAC. The *RF front-end* multiplies the modulating signal with the RF carrier, which results in a modulated RF signal. This signal is then amplified using a power amplifier (PA) and sent out to the antenna. After the PA, a bandpass filter (BPF) is often added to remove out-of-band distortion which results from nonidealities in the analog circuits.

The DAC and all analog components have a certain bandwidth, gain, linearity and power consumption. The design of a component consists in making the trade-off between these parameters. For example, if a very linear PA is to be designed, it is likely to consume more power than a PA with less stringent linearity specifications. Since different standards have different specifications for all of the above parameters, the trade-off between them has a different result for each standard. For example, one standard (e.g. GSM) may require the PA to have a very high gain while requiring less linearity, while another standard (e.g. WLAN) requires less gain but more linearity. Furthermore, the RF front-end, the PA, and the BPF are optimized for a specific carrier frequency. Therefore, different communication standards traditionally require different hardware.

The most straightforward way to implement a multistandard transmitter is by simply combining several transmitters, each of which is optimized for a different standard, as shown in Fig. [1.2.](#page-25-0) A global DSP block sends the data to one of these transmitters, while the others are turned off. As noted in [\[10\]](#page--1-8), this implementation is very power efficient since only the transmitter that is required is turned on, and it is optimized to satisfy the given standard with minimal power usage. However, implementing multiple parallel transmitters has a high area cost and requires a high

Fig. 1.2 Straightforward multistandard transmitter: multiple single-standard transmitters in parallel

Fig. 1.3 Multistandard transmitter with shared reconfigurable digital baseband and DAC

design effort. Furthermore, if an additional standard is to be added at a later time, this can only be done by adding or replacing hardware.

By implementing components in a more flexible way, they can be re-used for different standards. For example, in Fig. [1.3,](#page-25-1) all baseband components are made flexible and can be shared between the different standards. This means that e.g. the lowpass filter can be tuned to support different bandwidths. All RF components are still dedicated to a standard. This is a realistic situation since the RF components usually have to meet tougher specifications and are therefore less easily made flexible.

This work, however, aims at making the RF front-end flexible as well, as shown in Fig. [1.4.](#page-26-0) In this transmitter, there is only one flexible signal path that produces the RF signals for any supported communication standard. This implies that this path should support different carrier frequencies, bandwidths, and modulation schemes.

In order to achieve a fully flexible multistandard transmitter, the PA and the output filter also have to become flexible, as shown in Fig. [1.5.](#page-26-1) This challenge, in combination with achieving high output power, is a separate research field which is outside the scope of this book. While most modern PAs are still limited to a certain frequency band, these bandwidths are currently increasing up to hundreds of MHz [\[4,](#page--1-9) [7](#page--1-10)] or even more than a GHz [\[9\]](#page--1-11), so that a limited number of PAs can cover a

Fig. 1.4 Multistandard transmitter with shared reconfigurable digital baseband, DAC, and RF front-end

Fig. 1.5 Fully reconfigurable multistandard transmitter

wide frequency range. Thus, while multiple PAs are still needed, this does not mean a separate PA is needed for every standard.

It should be noted that while the transmitters shown in Figs. [1.3,](#page-25-1) [1.4,](#page-26-0) [1.5](#page-26-1) support multiple standards, they can only transmit one standard at the time. Transmitting multiple standards concurrently is required in many applications: For example, a user may want to answer an incoming phone call while a large file is being sent out over a WLAN or Bluetooth link. Such concurrent multistandard transmission is an additional problem, which can be solved by duplicating the reconfigurable parts of the transmit chain (e.g. 2 reconfigurable chains can be combined with 5 standard-dependent parts in order to transmit up to 2 out of 5 different standards simultaneously). Alternatively, a reconfigurable multi-channel transmitter can be designed which can simultaneously transmit multiple standards in a more efficient way. While this is an important issue in the design of multistandard transmitters, it is not the scope of this work.

The DSP block in Figs. [1.1,](#page-24-1) [1.2,](#page-25-0) [1.3,](#page-25-1) [1.4,](#page-26-0) [1.5](#page-26-1) can be a dedicated hardware block designed for signal processing, but it can also be some generic processor on which DSP software is running. If this is the case, new standards can be added to an existing transmitter by performing a software update, as long as the new standards fall within the ranges supported by the reconfigurable blocks. This is an example of *softwaredefined radio* (SDR).

1.1.2 Towards Fully Integrated CMOS Transceivers

There is a growing tendency to integrate as many components as possible on-chip for several reasons: First, on-chip components are much smaller, so that the overall size of the device can be reduced, or more functionality can be provided with the same size. Furthermore, chips can be produced at low prices provided that the volume (i.e. the number of produced chips) is high enough: The highest cost in CMOS production is the creation of the mask set. Once available, a mask set can be re-used to produce arbitrary numbers of chips at a very low cost, so that the price of a chip becomes inversely proportional to the number of chips that can be sold. Finally, when moving to multiple-GHz carrier frequencies, bringing signals off-chip can be a problem since bond wires, pins, printed circuit board (PCB) tracks, etc. typically act as lowpass filters. Therefore it is advantageous to keep signals on-chip as long as possible.

In the digital world, CMOS is a very popular technology due to its low manufacturing cost (for high volumes) and its very small transistor sizes which decrease continually while the speed keeps increasing. This allows providing ever increasing functionality on the same chip area. Furthermore, CMOS circuits typically have a low power consumption, which keeps decreasing with the transistor sizes and supply voltages.

In order to implement fully integrated single-chip transmitters, analog components, including RF front-ends and PAs, need to be integrated on the same chip as the digital baseband, which requires implementing them in CMOS as well. However, CMOS technologies are optimized for digital design and present several problems when used to implement analog circuits. First of all, the technologies are focused on miniaturization of transistors, while the passive components (resistors, capacitors and inductors) are generally very large compared to the transistors and furthermore have fairly low quality.

Furthermore, due to the extensive miniaturization, both active and passive devices on CMOS chips have high parasitic capacitances, which are generally undesired but cannot be avoided. In addition, deviations in the production process cause very large fluctuations in the parameters of active and passive devices. Analog circuits are more sensitive to this, which makes their exact behaviour unpredictable. These variations can be reduced by increasing the sizes of the components, but this reduces the benefits in terms of area and power consumption, so that scaling is much less beneficial for analog components.

Finally, due to the low supply voltages, it becomes increasingly difficult to achieve good voltage resolution and linearity. Furthermore, the output power that can be achieved by a CMOS amplifier is very limited and usually insufficient for wireless communication. Increasing the supply voltage is nontrivial as the very small transistors are not suited for high voltages and may break down if too high a voltage is applied across them. Therefore, high-voltage circuits require either special transistors, which are larger and more expensive, or special design techniques to limit the voltages across every individual transistor. Furthermore, scaling transistor sizes

without scaling the voltage results in a quadratic increase of the on-chip power density (i.e. the dissipated power per unit area) [\[11](#page--1-12), Sect. [3.5\]](http://dx.doi.org/10.1007/978-3-319-03925-1_3), which would very soon result in cooling problems and degradation of the transistors.

All these issues make the implementation of fully integrated CMOS transmitters a challenge of its own. Clearly, it is advantageous to implement as many parts as possible in the digital domain, since this way they can better exploit the benefits of CMOS technology scaling.

1.1.3 Switched-Mode Power Amplification

Switched-mode power amplifiers (SMPAs) are power amplifiers (PAs) that switch between two discrete voltage levels rather than amplifying continuous signals. SMPAs are gaining popularity for several reasons. First, they are more efficient than traditional linear PAs (e.g. classes A, AB, B, and C): In theory they can achieve efficiencies up to 100% [\[13](#page--1-13)], which is not the case for linear PAs.

Furthermore, since SMPAs switch between only two levels, they are inherently linear and do not suffer from any nonlinearities in the transistors that are used or from the limited supply voltages. This makes them suitable for integration on CMOS chips.

However, the limitation to two discrete voltage levels also implies a major disadvantage. Frequency modulation (FM) or phase modulation (PM) signals can be amplified without problems by replacing the sinusoidal carrier with a square wave. The sinusoidal shape is restored in or after the PA by bandpass filtering. However, amplitude modulation (AM) cannot be applied since the PA is not capable of producing any intermediate levels.

While many communication standards are based only on FM or PM precisely to avoid any voltage nonlinearity issues and enable the use of nonlinear PAs, many modern standards include AM in order to achieve higher data rates. In order to implement such standards using SMPAs, the complete signal, including AM, needs to be encoded into a single-bit digital signal.

Many transmitter implementations, especially in modern CMOS technologies, use multiple PAs in parallel whose outputs are connected to a power combiner [\[3](#page--1-14)[–5,](#page--1-15) [7,](#page--1-10) [14,](#page--1-16) [18](#page--1-17)]. In this case, one could drive the PAs with different signals so that more than two signal levels can be used. This facilitates the implementation of amplitude modulation. Nevertheless, the RF signal before the PA will be limited to a very small set of discrete values.

While the focus of this book is on the RF front-end rather than on the PA, it is assumed that the implemented transmitters use one or more SMPAs, and the design of the circuits presented in this work is based on this assumption.

1.1.4 Towards Fully Digital Transmitters

The previous sections stated several requirements that occur frequently in modern transmitters:

- The components should be reconfigurable in order to support multiple standards.
- They should be fully integrated, preferably in CMOS.
- They should be able to drive an SMPA while still supporting AM signals.

All these specifications lead to the desire to implement as many components as possible in the digital domain. First, digital circuits consist mostly of logical gates and can therefore easily be made reconfigurable by adding more gates and some control signals. Thus they are more flexible than analog circuits.

Furthermore, as mentioned in Sect. [1.1.2,](#page-27-1) CMOS technologies are much more suited to implement digital circuits than analog circuits. Digital circuits use few or no passive components and do not suffer from the low supply voltages. Their performance improves every year due to the area reduction and speed increase of CMOS transistors. Digital circuits are also much less sensitive to process variations than analog circuits. This way, digital circuits fully exploit the benefits of CMOS while being relatively immune against its disadvantages.

Finally, digital circuits are ideal to produce the single-bit signals required to drive SMPAs. While AM cannot be directly included in such signals, digital circuits can use their high speeds to encode this information in the time domain, as will be demonstrated in this work. When an SMPA is driven directly from the digital domain, the DAC can be removed and all signals are represented using discrete voltage levels up to the PA. Thus, the only place where voltage linearity still matters is in the output bandpass filter.

Figure [1.6](#page-30-1) shows such a transmitter architecture, which is an improved version of the *software-defined radio* (SDR) transmitter. The DAC and the lowpass filter have been removed and the RF front-end has been replaced by a so-called digital RF frontend. This front-end still converts the baseband signal to RF but does so in a completely digital way, i.e. using only two-level signals. It produces a digital RF signal which directly drives the SMPA. Since there are now fewer analog components, the transmit chain is more reconfigurable and can more easily support multiple communication standards. Furthermore, it does no longer depend on voltage linearity which makes it more robust against technology scaling. As will be shown using simulation results in Sects. [3.4](http://dx.doi.org/10.1007/978-3-319-03925-1_3) and [3.6,](http://dx.doi.org/10.1007/978-3-319-03925-1_3) and using measurement results in Sect. [3.6,](http://dx.doi.org/10.1007/978-3-319-03925-1_3) this type of circuits will actually benefit from technology scaling.

The digital RF front-end consists of dedicated components which are flexible but designed specifically to produce a modulated RF carrier. A more extreme form of digitization is shown in Fig. [1.7.](#page-30-2) Here, the whole RF front-end has been absorbed into a generic DSP block which can e.g. be a processor with DSP software. In this case, the signal that goes to the PA is entirely determined by software, and there is even more flexibility to add new standards after the circuit has been produced. This type of transmitter is called *software radio* (SR). Ideally, the PA and output filter

Fig. 1.6 Fully digital reconfigurable multistandard transmitter

Fig. 1.7 Software radio transmitter

would also be incorporated in the digital block and replaced with a DAC. However, as explained in [\[8,](#page--1-18) [10\]](#page--1-8), it is not feasible to implement such transmitters with the technologies that are currently available due to the high sampling rates that would be required to oversample the RF signal, and (in case the PA is also digitized) the high output power that is required.

This book focuses on the transmitter architecture shown in Fig. [1.6,](#page-30-1) and more specifically on the digital reconfigurable RF front-end.

1.1.5 The Bandpass Filter

Figures [1.1,](#page-24-1) [1.2,](#page-25-0) [1.3,](#page-25-1) [1.4,](#page-26-0) [1.5,](#page-26-1) [1.6,](#page-30-1) [1.7](#page-30-2) all show a bandpass filter (BPF) before the antenna. This filter is often required in order to reduce the power that is transmitted outside the frequency band where the communication takes place. Standards often include hard specifications about such *out-of-band power*, since this power may be located in the frequency bands used for other communication standards or other channels of the same communication standard, and thus disturb the communication in those frequency bands.

The amount of filtering that is required depends on the transmitter architecture that is used: As will be shown in Chap. [2,](http://dx.doi.org/10.1007/978-3-319-03925-1_2) some architectures produce more out-ofband power than others, and the frequencies where this power is located also depend on the architecture. Generally, digital architectures produce more out-of-band power than analog ones due to the voltage quantization.

In general, PAs and antennas are band-limited and thus inherently perform some bandpass filtering. In addition, an on-chip bandpass filter can be added if needed. However, these types of filtering are usually relatively weak, and furthermore on-chip filters are normally realized using passive components which take a lot of area.

Much stronger filtering can be achieved using off-chip filters, which can either be implemented with off-chip passive components which have much higher quality, or using mechanical filters such as *surface acoustic wave* (SAW) filters. However,

such filters are expensive, take up a lot of space, and cannot be reconfigured so that a separate filter is needed for each frequency band. This makes them undesirable or even unacceptable in many applications, especially those that need to be small, cheap, and support multiple standards, such as smartphones.

Therefore, while the design of the bandpass filters themselves is outside the scope of this book, the amount and shape of out-of-band power will be considered an important criterion throughout this work.

1.1.6 Frequency Range

Many modern communication standards (e.g. GSM, LTE and some of the WLAN bands) use frequencies ranging from around 900 MHz to several GHz. Therefore, this work targets carrier frequencies from 900 MHz to about 3 GHz. Since the performance of the presented type of transmitters decreases with frequency, higher frequencies would currently result in insufficient performance. However, since the performance directly depends on transistor speed, this will improve with technology scaling.

1.1.7 Continuous-Time Digital Circuits

Figure [1.8](#page-32-0) illustrates several ways of representing signals. Figure [1.8a](#page-32-0) shows a *continuous-time analog signal x*(*t*) (also known simply as an *analog signal*), which is a continuous function of time: At each instant *t*, the signal has a certain value $x(t)$, which is most often a voltage or current. This value can change at any moment and it can have any value within a continuous range.

In order to facilitate circuit design and improve the robustness of the circuits, one or two dimensions on this plot can be discretized, i.e. limited to a discrete set of values. Figure [1.8b](#page-32-0) shows a *continuous-time digital signal*, which results from *quantizing* the analog signal to a limited set of *quantization levels*. At every instant *t*, the signal is now rounded to the nearest quantization level. Thus, the time dimension is still continuous, but the values of the signal are now discrete. The quantization levels are usually spaced equidistantly, where the distance *q* is called the *quantization step*.

Figure [1.8c](#page-32-0) shows a *discrete-time analog signal*, which results from *sampling* the analog signal using a *sample-and-hold* device. The signal can still assume a continuous range of values but can only change at discrete points in time, which are usually spaced equidistantly and separated by the *sampling period Ts*. The sampleand-hold device samples the signal at every sampling instant kT_s (where k is an integer) and then keeps the value constant during the whole period. The sample-andhold block is usually triggered by a *clock signal*, which is a square wave at frequency $f_s = 1/T_s$, which is called the *sampling frequency* or *sampling rate*.

Fig. 1.8 Illustration of the difference between signal representations depending on whether the time and the signal amplitude are continuous or discrete. **a** Continuous-time analog, **b** Continuous-time digital, **c** Discrete-time analog, **d** Discrete-time digital

If an analog signal is both quantized and sampled, the result is a traditional *discrete-time digital signal* (also known simply as a *digital signal*), as shown in Fig. [1.8d](#page-32-0). Now both the time and the value are discretized and the signal is restricted to a rectangular grid: at every sampling instant kT_s , the analog signal is sampled and rounded to the nearest quantization level.

Continuous-time analog and discrete-time digital signals are the most known types, as they are used in traditional analog and digital circuits, respectively. The other two signal types are less known but are also used in certain applications. Discrete-time analog signals occur e.g. in *switched-capacitor* circuits [\[1](#page--1-19)]. Continuous-time digital signals occur in *time-to-digital* [\[2](#page--1-20)] and *digital-to-time converters*, which often serve as subblocks for implementing *analog-to-digital* and *digital-toanalog converters*.

As explained in Sect. [1.1.4,](#page-29-1) there are many reasons to prefer digital circuits in the context of this work. However, Sects. [1.1.3](#page-28-1) and [1.1.4](#page-29-1) explained that for the targeted systems the RF output signal must be encoded into only 1 or in any case very few bits. Nevertheless, it needs to be represented accurately in order to allow high data rates to be transmitted without introducing bit errors. These requirements seem to be contradictory.

However, if the position of the signal edges can be accurately controlled, the quantization noise resulting from the low number of signal levels can be moved to higher frequencies, while the low-frequent part of the signal still contains the