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High Speed and Wide Bandwidth Delta-Sigma ADCs

Springer

Analog Circuits and Signal Processing

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ISSN 1872-082X
ISBN 978-3-319-05839-9
DOI 10.1007/978-3-319-05840-5
ISSN 2197-1854 (electronic)
ISBN 978-3-319-05840-5 (eBook)
Springer Cham Heidelberg New York Dordrecht London

Library of Congress Control Number: 2014935880

Printed on acid-free paper

Springer is part of Springer Science+Business Media (www.springer.com)

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Chapter 1
Introduction

Analog-to-digital converter developments are driven by the increasing demand for signal bandwidth and dynamic range in applications such as medical imaging, high-definition video processing and, in particular, wireline and wireless communications. Figure 1.1 shows a block diagram of a basic wireless receiver. It has three main building blocks: an RF front-end, an analog-to-digital converter (ADC) and a digital baseband processor. The role of the RF front-end is to filter, amplify the signals present at the antenna input and down-convert them to baseband. The ADC samples and digitizes the analog signals at the output of the RF front-end and outputs the results to the baseband processor. To achieve high data rates, wireless standards rely on advanced digital modulation techniques that can be advantageously implemented in baseband processors fabricated in nanometer-CMOS, which also motivates the development of ADCs in these technologies.

In modern wireless applications such as digital FM and LTE-advanced, the ADC receives a signal whose bandwidth can be as large as 100 MHz [1–3]. A wideband ADC which can capture such signals simplifies the design of the RF front-end, since the channel selection filters can then be implemented in the baseband processor. However, due to the limited filtering characteristic of the RF front-end, large unwanted signals (blockers) are often present at the input of the ADC. Therefore, the ADC should have a high dynamic range, often more than 70 dB. Wide bandwidth and high dynamic range (DR) are thus important attributes of ADCs intended for high data-rate next-generation wireless applications.

Practically, Nyquist ADCs have been preferred for applications which target wide bandwidth, since the sampling frequency (f_s) only has to be slightly higher than $2 \times BW$, where BW is the bandwidth of the desired signal. A plot of dynamic range vs. bandwidth for various state-of-the-art ADCs with energy efficiency less than 1pJ/conv.-step. is shown in Fig. 1.2. As can be seen, many Nyquist ADCs achieve both wide bandwidths and high DR. A Nyquist ADC requires an input sampling circuit which is often implemented with a switched-capacitor network. Achieving high DR, then requires low thermal noise, which in turn, leads to a large

M. Bolatkale et al., *High Speed and Wide Bandwidth Delta-Sigma ADCs*, Analog Circuits and Signal Processing, DOI 10.1007/978-3-319-05840-5_1,

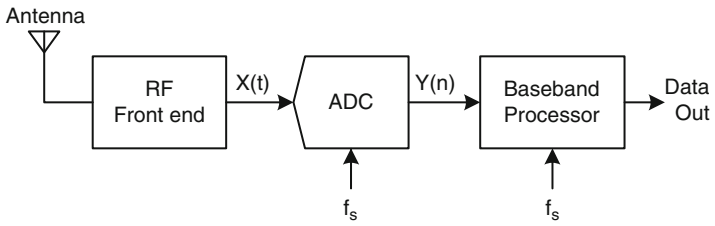

Fig. 1.1 A basic block diagram of a wireless receiver

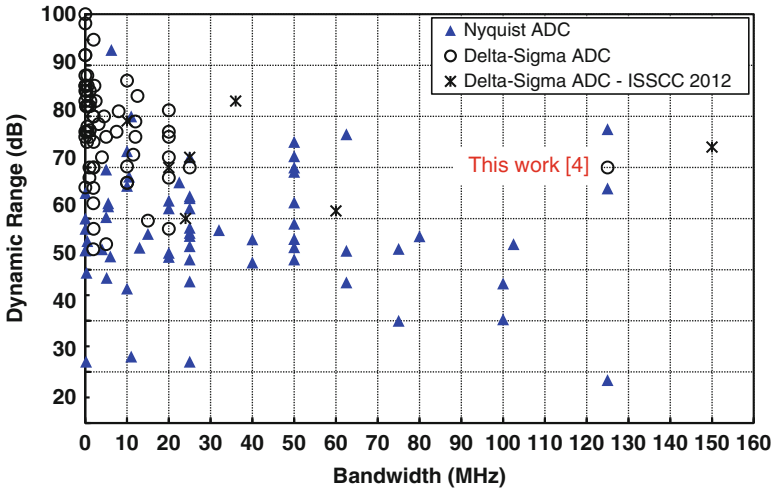

Fig. 1.2 Dynamic range vs. bandwidth of state-of-the-art ADCs with power efficiency less than 1 pJ/conv.-step. The high speed CT$\Delta\Sigma$ ADCs implemented in nm-CMOS that have recently gained popularity are included to emphasize the developments in oversampled converters [5]

input capacitance. However, this must be preceded by an anti-aliasing filter and an input buffer capable of driving a large capacitance, which increases the complexity and power of the RF front-end.

Oversampled converters are very well suited for applications which require high dynamic range. In particular, a delta-sigma modulator ($\Delta\Sigma$M), which trades time resolution for amplitude resolution, can achieve a high dynamic range with very good power efficiency (Fig. 1.2). The $\Delta\Sigma$M is one of the most promising converter architectures for exploiting the speed advantage of CMOS process technology. However, achieving a wide bandwidth with a $\Delta\Sigma$M requires a high-speed sampling frequency due to the large OSR ($f_s = 2 \times OSR \times BW$, where OSR is the oversampling ratio). The stability and power efficiency of the modulator at a high sampling rate, together with achieving a high dynamic range at the low supply voltages required by the nanometer-CMOS fabrication process, are important challenges that face the next generation of oversampled converters.

This book focuses on the design of wide-bandwidth and high dynamic range $\Delta\Sigma$Ms that can bridge the bandwidth gap between Nyquist and oversampled converters. More specifically, this book describes the stability, the power efficiency and the linearity limits of $\Delta\Sigma$Ms aiming at a GHz sampling frequency.

1.1 Trends in Wide Bandwidth and High Dynamic Range ADCs

As shown in Fig. 1.2, Nyquist ADCs based on the pipeline architecture have achieved sampling speeds of up to 125 MHz and dynamic ranges greater than 70 dB in standard CMOS [6–8]. To achieve higher sampling rates, a Bi-CMOS or SiGe Bi-CMOS process can be used at the cost of higher power consumption due to their higher supply voltages (1.8–3.0 V) [9, 10]. A further drawback of pipeline ADCs is that they typically rely on high-gain wideband residue amplifiers and/or complex calibration techniques to reduce gain errors [7–9], thus increasing their area and complexity.

Recently, Nyquist ADCs based on the successive approximation register (SAR) architecture have achieved signal bandwidths of up to 50 MHz with 56–65 dB DR and excellent power efficiency (<80 fJ/conv.-step) [11–14]. Greater bandwidth can be achieved by using time-interleaving. However, the linearity of time-interleaved SAR ADCs is limited by gain, offset, and timing errors and so such ADCs also require extensive calibration [15]. Furthermore, time interleaving increases input capacitance and chip area, and thus places more demands on the input buffer [16].

By contrast, CT$\Delta\Sigma$ ADCs can have a simple resistive input that does not require the use of a power-hungry input buffer or an anti-aliasing filter, which further relaxes the requirements of the RF front-end. When implemented in CMOS, such ADCs have achieved signal bandwidths of up to 25 MHz with a 70–80 dB dynamic range and good power efficiency (<350 fJ/conv.-step) [17–19]. Typical CT$\Delta\Sigma$ modulators employ a high-order loop filter with a multi-bit quantizer, which, for a 20 MHz bandwidth, require sampling frequencies of 0.5–1 GHz to achieve more than 70 dB of dynamic range. Assuming that the sampling frequency is proportional to the bandwidth, sampling frequencies of 2.5–5 GHz will be then required to achieve bandwidths greater than 100 MHz. However, at GHz sampling rates, parasitic poles and quantizer latency can easily cause modulator instability.

CT$\Delta\Sigma$ modulators with signal bandwidths up to 20–25 MHz have been implemented in 90–130 nm CMOS. The switching speed of an NMOS transistor in 45 nm CMOS is approximately 1.6× faster than in 90 nm CMOS and 2.7× faster than in 130 nm CMOS[20]. Implementing a $\Delta\Sigma$ modulator in 45 nm LP CMOS is thus advantageous for circuits such as quantizers and DACs whose delay is important for stability. However, the dynamic range of circuits in 45 nm CMOS is limited by the low intrinsic gain and poor matching of the transistors [21, 22]. The low operating supply (1.1–1.0 V) furthermore implies that cascaded stages are required

to make gain in blocks such as an OTA or a quantizer. Therefore, the intrinsic speed of 45 nm LP CMOS cannot be fully utilized. To realize CT$\Delta\Sigma$ modulators with bandwidths greater than 100 MHz in CMOS, innovations are still required at the system-level design. A comparison of ADC architectures targeting wide bandwidth (BW $>$ 100 MHz) and high dynamic range (DR $>$ 70 dB) is presented in Appendix A.

1.2 Motivation and Objectives

The $\Delta\Sigma$M is an architecture which trades time resolution (signal bandwidth) for amplitude resolution, or in other words, dynamic range. Wide bandwidth and high dynamic range $\Delta\Sigma$Ms have received much attention since every new generation of CMOS process technology brings a speed advantage.[1] The fundamental limitations of a single-loop CT$\Delta\Sigma$ modulator targeting a wide bandwidth and a high dynamic range define the scope of this book.

The aim of the research described in this book is to develop a wideband, high dynamic range $\Delta\Sigma$M which demonstrates that an oversampled converter can also cover the application space where Nyquist ADCs are currently preferred. Furthermore, such a $\Delta\Sigma$M should also achieve state-of-the-art power efficiency. This quest is achieved by tackling the research question both at the system and circuit level.

A $\Delta\Sigma$M is a non-linear system, and often the design trade-offs are hidden behind complex system-level simulations. Therefore, system-level understanding of the modulator is required to find architectural solutions. The stability of a $\Delta\Sigma$M is a very important aspect of its design. As the sampling speed of the modulator increases to achieve more bandwidth, second order effects such as the limited unity gain bandwidth of amplifiers and the limited switching speed of the transistors start effecting the modulator's stability. One of the main research goals of this book is to find system level solutions that enable the design of a wide bandwidth, high dynamic range modulator with state-of-the-art power efficiency.

Theoretically, it is possible to design a stable $\Delta\Sigma$M for any given specification [30]. However, practical limitations at the circuit level define the possible solutions that can be implemented. For example, the limited speed of the transistors introduces excess loop delay (ELD) which degrades the stability of the modulator, and at GHz sampling frequencies, ELD limits the performance. Such practical limitations might be solved by dissipating more power, although this does not prove that a stable $\Delta\Sigma$M with desired specifications can be implemented. As a second objective of this book, we explore the circuit-level design techniques to assist the proposed system-level design solutions and push the design boundary of the oversampled converters in terms of dynamic range, bandwidth, linearity, and power efficiency.

[1] Recently, high speed CT$\Delta\Sigma$ ADCs implemented in nm-CMOS have gained popularity [23–29].

To demonstrate the feasibility of the ideas and approaches presented in this book, we have designed and implemented a CT$\Delta\Sigma$ with a bandwidth (BW) greater than 100 MHz and a dynamic range above 70 dB in nm-CMOS. This is achieved by using a low oversampling ratio and multi-bit architecture. The performance of a multi-bit CT$\Delta\Sigma$ is often limited by the dynamic errors at GHz sampling rates, and the correction/calibration techniques that are applicable are bounded by the stability requirements. To overcome these limitations, we have implemented a dynamic error correction technique which not only experimentally quantifies the level of dynamic errors but also improves the dynamic performance of the modulator.

1.3 Organization of the Book

Chapter 2 starts with a brief description of an ideal single-loop $\Delta\Sigma$M. The building blocks of the modulator are analyzed and their characteristic properties are discussed to provide a basic understanding of the modulator's operation. The stability of the $\Delta\Sigma$M is discussed and the relation between this and the main building blocks is presented. Moreover, this chapter discusses the system-level non-idealities in a $\Delta\Sigma$M such as noise, nonlinearity, metastability and ELD. The understanding of the system-level non-idealities is especially important to achieve the optimum performance for a given $\Delta\Sigma$M architecture.

Chapter 3 focuses on the design of CT$\Delta\Sigma$ modulators aiming at GHz sampling frequencies. The system-level non-idealities discussed in Chap. 2 pose a major limitation at these frequencies, and limit the possible architectural implementations. In this chapter, we present the system-level trade-offs in a single-loop $\Delta\Sigma$M and propose a 3rd order multi-bit $\Delta\Sigma$M which can achieve an 80 dB signal-to-quantization noise ratio (SQNR) in a 125 MHz BW with a sampling rate of 4 GHz. Mitigating ELD and metastability are crucial to meet the target sampling rate, therefore we present a high speed modulator architecture which overcomes the limitation of the summation amplifier present in high speed modulators, and improves its power efficiency. Furthermore, we present the block-level design requirements of the proposed architecture. Each building block is analyzed based on its most important non-ideality and block-level specifications are listed.

Chapter 4 describes the implementation details of a 4 GHz CT$\Delta\Sigma$ ADC which uses the high-speed modulator architecture proposed in Chap. 3. The ADC is implemented in 45 nm-LP CMOS and achieves a 70 dB DR and -74 dBFS total harmonic distortion (THD) in a 125 MHz BW. Since the clocking scheme of the quantizer and feedback DACs is crucially important for the stability of the modulator, this chapter presents a detailed timing diagram of the modulator. The implemented ADC is characterized by using a custom measurement setup, and the detailed measurement results are presented particularly focusing on the jitter performance of the ADC.

Chapter 5 explains a 2 GHz CT$\Delta\Sigma$ ADC where dynamic errors of its multi-bit digital-to-analog converter (DAC) are masked by using an error switching

(ES) scheme at the virtual ground node of the first integrator. This technique prevents the loop filter from processing the dynamic errors in the feedback DAC and improves the signal-to-noise ratio (SNR), signal-to-noise-and-distortion ratio (SNDR), and THD of the modulator. This chapter also explains the design and implementation of a multi-mode version of the high-speed architecture presented in Chap. 4. Furthermore, a high-speed error sampling switch driver is discussed and detailed measurement results are presented.

Finally, **Chap. 6** concludes this work and suggests future research directions based on the insight gained during this research.

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