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CMOS RF Circuit Design for Reliability and Variability

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Chapter 1
Introduction

It is well known that wireless transceivers are implemented in mobile devices such as smart phones, laptops, tablets, etc. Wireless transceivers are also critical circuit blocks for sensors in the Internet of Things (IoT) era. IoT is being represented as a worldwide network interconnecting things/objects. IoT is a kind of technology that realizes the communication and information exchange between machine and human and machine by embedded RFID, GPS, and sensors technologies into physical equipment, and achieve transition, cooperation, processing of information according to some protocols and so that achieve the goal of intelligent identification, tracking, monitoring, computing, and management. IoT is made up of sensing layer, network layer, and application layer. Sensing layer is responsible for accumulation of data and information. Network layer realizes the management of connection of network and data and transmits information to application layer. Application layer processes information in order to realize monitoring, identification, control, and other functions. Network layer mainly guarantees the connection of network. It can support the network protocols of internet and provide efficient channel for voice and data. To sum up, IoT is a combination of many kinds of networking technologies, and at the same time, IoT cannot be developed without the support of communication network.

Clearly, wireless technologies are very important in IoT area due to the convenient and low cost wireless connections between IoT nodes. RF transceiver is the critical block in wireless nodes and consumes the majority of energy. A typical super-heterodyne architecture transceiver is widely used in RF transceivers with better sensitivity and higher gain. For a super-heterodyne topology in RF transceiver, for example in the receiver (RX) path, the RF signal coming from the antenna and RF switch goes to the front-end low-noise amplifier (LNA). The RF signal is amplified by the LNA and down converted to the intermediate frequency (IF) signal using the mixer and local oscillator (LO). The IF signal then passes through the analog-to-digital (A/D) converter for base band digital signal processing. On the other hand, for the transmitter (TX) path, the digital signal passed through the digital-to-analog (D/A) converter to produce the analog signal. The IF

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is then up-converted to RF signal using the up-converting mixer and LO at desired frequency. The RF signal is amplified by the power amplifier (PA). The RF switch connects the large-signal RF waveform to the antenna for signal transmission.

RF transceiver circuits including low noise amplifiers, mixers, oscillators, and power amplifiers are usually made using mixed-signal CMOS technology. CMOS is an ideal candidate for high density, low cost, low power, and high integration chip solution. Today, silicon CMOS are scaled down to 22 nm and beyond to increase density and performance further. The well-known reliability mechanisms such as hot carrier injection (HCI), negative bias temperature instability (NBTI), and gate oxide breakdown (GOB) become very important knowledge for the design of advanced RF and digital circuits. For state-of-the-art nanoscale circuits and systems, the local device variation and uncertainty of signal propagation time have become crucial in the determination of system performance and reliability. Yield analysis and optimization, which take into account the manufacturing tolerances, model uncertainties, variations in the process parameters, and aging factors are known as indispensable components of the circuit design procedure. Therefore, circuit designers, device engineers, and graduate students need to have clear understanding on how device reliability issues affect the RF circuit performance subjected to operation aging and process variations. This book is unique to explore typical reliability issues in the device and technology level and then to examine their impact on RF wireless transceiver circuit performance. Analytical equations, experimental data, mixed-mode device, and circuit simulation results will be given for clear illustration.

Chapter 2
CMOS Transistor Reliability and Variability Mechanisms

Due to aggressive scaling in device dimensions for improving speed and functionality, CMOS transistors in the nanometer regime have resulted in major reliability issues due to high electric field phenomenon. These include hot carrier injection (HCI) [1, 2], gate oxide breakdown (BD) [3, 4], and negative bias temperature instability (NBTI) [5, 6]. These reliability mechanisms cause the MOS transistor parameter drifts; namely, threshold voltage shift and mobility degradation. A brief discussion on the MOS device reliability is described as follows.

2.1 Hot Electron Effect

When the electric field at the drain edge of the MOS transistor is very high, avalanche breakdown may occur. Impact ionization in the drain depletion region generates many energized electrons. These high energy carriers may damage interfacial layer and create interface traps and oxide trapped charges [7] which degrade device parameters such as an increase in threshold voltage. Figure 2.1 displays the drain current degradation versus drain-source voltage subjected to different stress times. At given drain-source voltage V_{DS} and gate-source voltage V_{GS}, the drain current decreases with stress time as shown in Fig. 2.1.

2.2 Gate Oxide Breakdown

High electric field across the gate insulator could induce time-dependent dielectric breakdown. The formation of random defects and conduction path within the gate dielectric increases the gate leakage and noise. For ultrathin gate oxide transistors under constant gate voltage stress, the soft breakdown could be observed before hard breakdown [8]. Compared with hard breakdown (HBD), SBD becomes more

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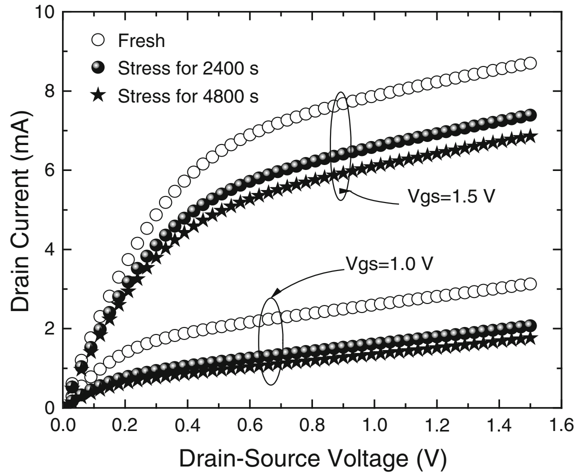

Fig. 2.1 Drain current degradation due to hot electron stress (© IEEE)

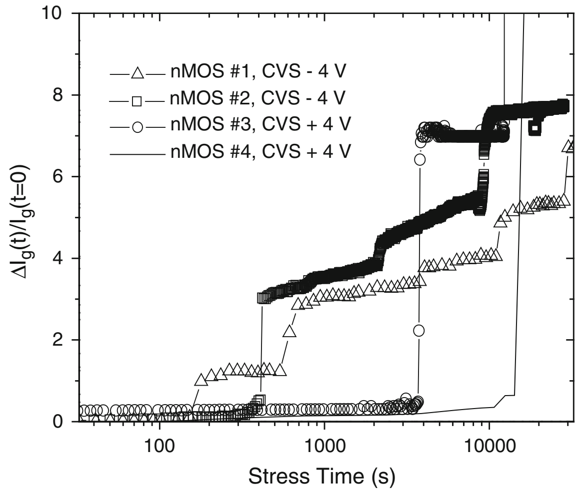

Fig. 2.2 Normalized I_g versus stress time. The nMOS is under positive or negative constant gate bias (© IEEE)

prevalent for thinner oxides and for oxide stress at relatively lower voltages. In addition, hot carrier injection could trigger more SBD in addition to conventional Fowler–Nordheim (FN) tunneling [9].

Figure 2.2 shows the normalized gate leakage current as a function of stress time under constant voltage (CVS). The gate soft breakdown degrades the threshold voltage and mobility of the MOSFET as observed by the current–voltage characteristics [10].