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Multiple Constant Multiplication Optimizations for Field Programmable Gate Arrays

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With a preface by Prof. Dr.-Ing. Peter Zipf

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Martin Kumm
Kassel, Germany

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Preface

As silicon technology advances, field programmable gate arrays appear to gain ground against the traditional ASIC project starts, reaching out to form the mainstream implementation basis. Their predefined structures result in an essential inefficiency, or performance gap at all relevant axes, i.e. clock frequency, power and area. Thus, highly optimised system realisations become more and more important to use this technology at its best. Microarchitectures and their adaptation to the FPGA hardware, combined with an optimal matching of model structures and FPGA structures, are two points of action where engineers can try to get optimally balanced solutions for their designs, thus fighting the performance gap towards the ASIC reference.

While microarchitecture design based on the knowledge of FPGA structures is located in the domain of traditional hardware engineering, the mapping and matching is based on EDA algorithms and thus strongly related to computer science. Algorithms and the related sophisticated tools are permanently in short supply for leading edge optimisation needs.

Martin's dissertation deals with the algorithmic optimisation of circuits for the multiplication of a variable with constants in different flavours. As this type of operations is elementary in all areas of digital signal processing and also usually on the critical path, his approaches and results are of high relevance not only by themselves but also as a direction for further research. His direct contributions are the advancement of algorithmic treatment of pipeline-based multiplier circuits using heuristics and exact optimisation algorithms, the adaptation of several algorithms to the specific conditions of field programmable gate arrays, specifically lookup-table based multipliers, ternary adders and embedded multipliers with fixed word length, and the transfer of his findings to a floating-point multiplier architecture for multiple constants.

Along with all the accompanying details, this is a large range of topics Martin presents here. It is an impressive and comprehensive achievement, convincing by its depth of discussion as well as its contributions in each of the areas.

Martin was one of my first PhD candidates. Thrown into the cultural conflict between computer science and electrical engineering he soon developed a sense for the symbiosis of both disciplines. The approach and results are symptomatical for this developing interdisciplinary area, where systems and their optimisation algorithms are developed corporately.

I found Martin's text exciting to read, as it is a comprehensive work within the ongoing discussion of algorithmic hardware optimisation. His work is supported by a long list of successful publications. It is surely a contribution worth reading.

Kassel, 22. of April, 2016 *Prof. Dr.-Ing. Peter Zipf*

Abstract

Digital signal processing (DSP) plays a major role in nearly any modern electronic system used in mobile communication, automotive control units, biomedical applications and high energy physics, just to name a few. A very frequent but resource intensive operation in DSP related systems is the multiplication of a variable by several constants, commonly denoted as multiple constant multiplication (MCM). It is needed, e. g., in digital filters and discrete transforms. While high performance DSP systems were traditionally realized as application specific integrated circuits (ASICs), there is an ongoing and increasing trend to use generic programmable logic ICs like field programmable gate arrays (FPGAs). However, only little attention has been paid on the optimization of MCM circuits for FPGAs.

In this thesis, FPGA-specific optimizations of MCM circuits for low resource usage but high performance are considered. Due to the large FPGA-specific routing delays, one key for high performance is pipelining. The optimization of pipelined MCM circuits is considered in the first part of the thesis. First, a method that optimally pipelines a given (not necessary optimal) MCM circuit using integer linear programming (ILP) is proposed. Then, it is shown that the direct optimization of a pipelined MCM circuit, formally defined as the pipelined MCM (PMCM) problem, is beneficial. This is done by presenting novel heuristic and optimal ILP-based methods to solve the PMCM problem. Besides this, extensions to the MCM problem with adder depth (AD) constraints and an extension for optimizing a related problem – the pipelined multiplication of a constant matrix with a vector – are given.

While these methods are independent of the target device and reduce the number of arithmetic and storage components, i. e., adders, subtracters and pipeline registers, FPGA-specific optimizations are considered in the second part of the thesis. These optimizations comprise the inclusion of look-up table (LUT)-based constant multipliers, embedded multipliers and the use of ternary (3-input) adders which can be efficiently mapped to modern FPGAs. In addition, an efficient architecture to perform MCM operations in floating point arithmetic is given.

Acknowledgements

First of all, I would like to thank my supervisor, Prof. Dr.-Ing. Peter Zipf, who gave me the opportunity to do my PhD under his supervision. He provided an excellent guidance and was always open-minded to new and exceptional ideas, leading to creative and fruitful discussions. I also thank my colleagues at the digital technology group of the University of Kassel. In special, Michael Kunz, who had many ideas how to prepare the course material and Konrad Möller, who started as student with his project work and master's thesis and is now a highly-valued colleague. Our mathematicians, Diana Fanghänel, Dörthe Janssen and Evelyn Lerche, were always open to help with math related questions. The deep understanding in discrete optimization and ILP (and more) of Diana Fanghänel helped a lot in obtaining some of the results in this work. I am grateful to all the students that contributed to parts of this thesis with their bachelor or master's thesis, project work or student job: Martin Hardieck, who did a great job in the C++ implementation of RPAG extensions for ternary adders and the constant matrix multiplication (and the combination of both) during his project work, his diploma thesis and his student job; Katharina Liebisch, for implementing MCM floating point units for reference; Jens Willkomm, who realized the ternary adder at primitive level for Xilinx FPGAs during his project work; and Marco Kleinlein, who implemented flexible VHDL code generators based on the Floating Point Core Generator (FloPoCo) library [1]. I would also like to thank our external PhD candidates Eugen Bayer and Charles-Frederic Müller for interesting discussions and collaborative work. I also appreciate the financial support of the German research council which allowed me to stay in a post-doc position in Kassel.

During the PhD, I started cooperations with Chip Hong Chang and Mathias Faust from the Nanyang Technological University, Singapore, Oscar Gustafsson and Mario Garrido from the University of Linköping, Sweden, and Uwe Meyer-Baese from the Florida State University, USA. Especially, I am very grateful to Oscar Gustafsson to invite me as guest researcher in his group. Exchanging ideas with people from the same field expanded my horizon enormously. Thanks to the ERASMUS program, two visits in

Linköping were possible and further visits are planned. Another big help was the friendly support of other researchers. Levent Aksoy was always fast in answering questions, providing filter benchmark data or even the source code of their algorithms. My thanks also go to Florent de Dinechin and all the contributors of the FloPoCo library [1] for providing their implementations as open-source [2]. Open-source in research simplifies the comparison with other work which inspired me to publish the presented algorithms as open-source, too.

Last but not least, I want to kindly thank my wife Nadine and my son Jonathan. Their love and support gave me the energy to create this thesis.

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